Performance of two ASICs for astronomical CCD controller: SPA and CDA

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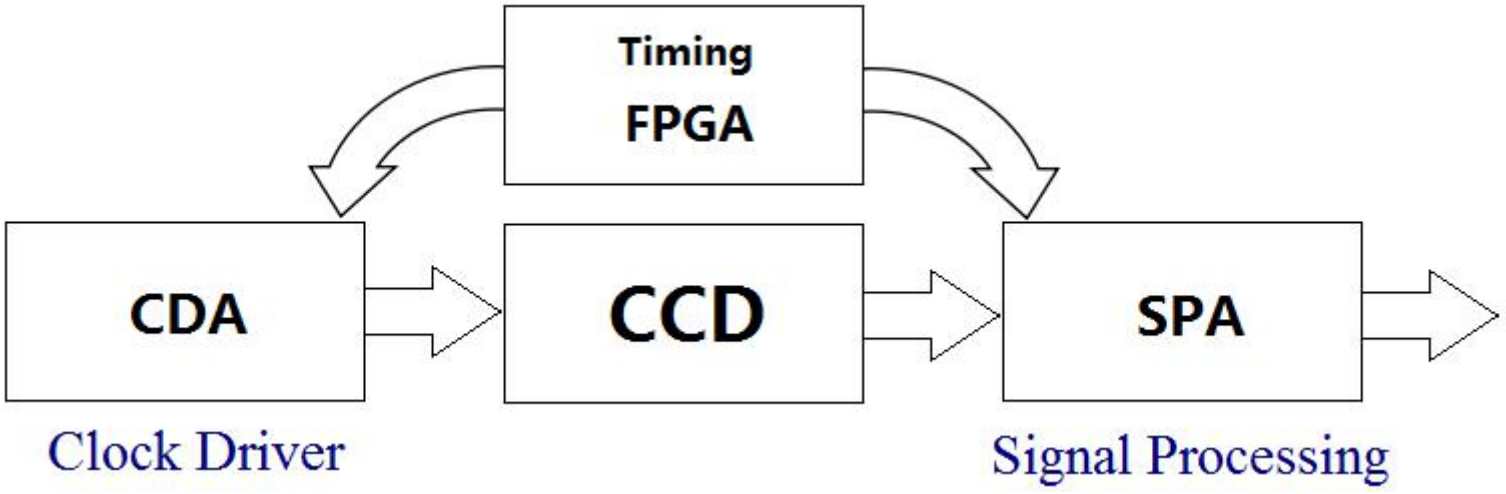
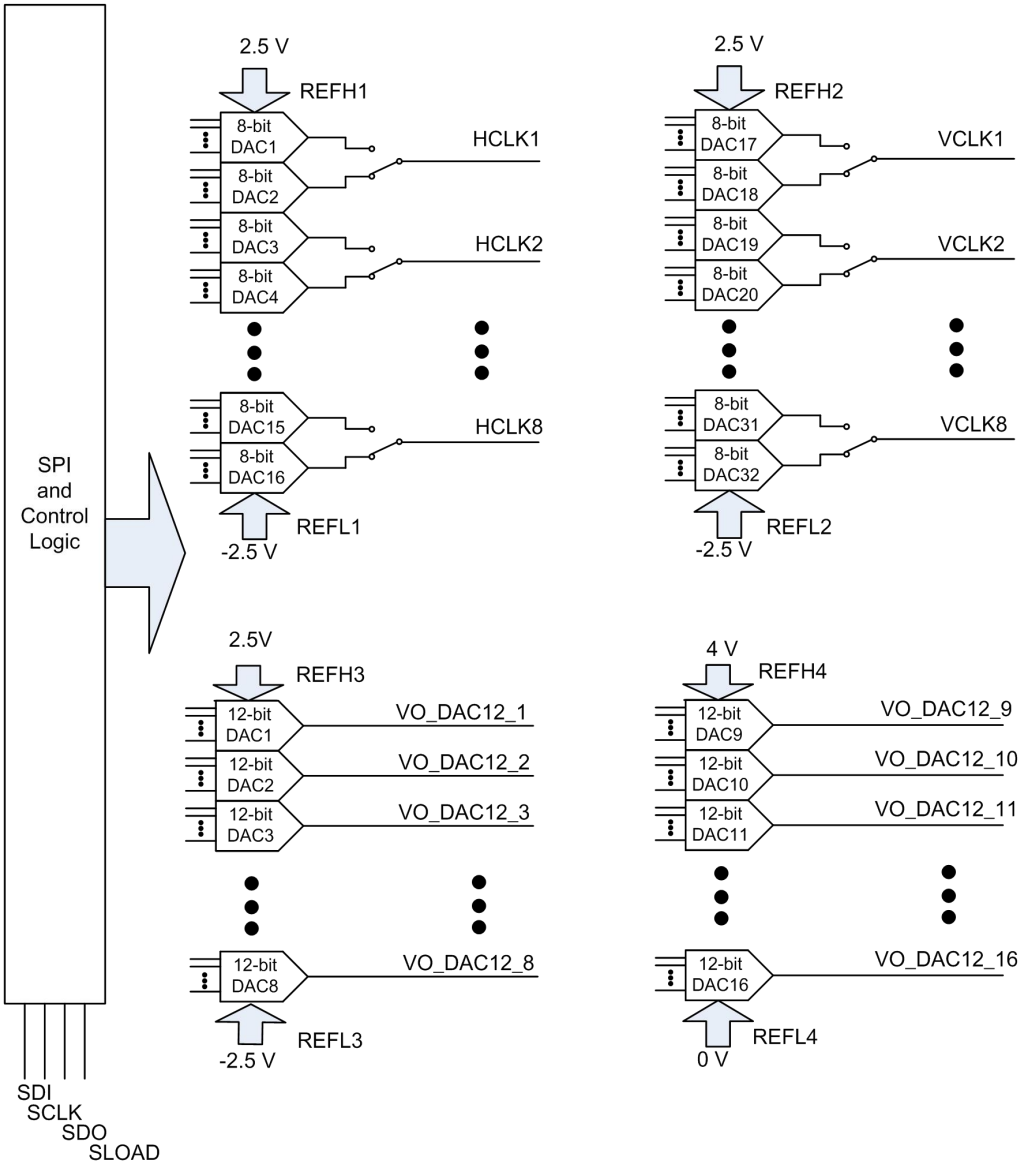


CCD controller system diagram

The Bias and Clock Drive ASIC for Astronomical CCD Controller (CDA)

The package of CDA2 (QFP144)



The main circuit block diagram of CDA

- **32** 8-bit DACs
  (for clocks)
  Switching Frequency≤20MHz
- **16** 12-bit DACs
  (for bias voltages)
- ±5V double power supply
- Linearity
  (-1 LSB<DNL<1 LSB)
- SPI Control Logic
- High voltage CMOS process