9. External Memory Interfaces in Cyclone III Devices

CIII51009-1.3

Introduction

In addition to an abundant supply of on-chip memory, Cyclone® III devices can easily interface to a broad range of external memory including DDR2 SDRAM, DDR SDRAM, and QDRII SRAM. External memory devices are an important system component of a wide range of image processing, storage, communications, and general embedded applications.

Cyclone III devices are supported with a comprehensive infrastructure to create robust external memory interfaces.

Table 9–1 highlights the major benefits of Cyclone III external memory interfaces.

Table 9–1. Major Benefits of Cyclone III Memory Interfaces

Benefit	Cyclone III Solution Description
Robust	Self-calibrating to adjust for process, voltage, and temperature changes.
Easy to use	■ Push button timing closure ■ DDR2/DDR available on all sides to ease PCB layout constraints ■ Half-rate solution available to lower f_{MAX} requirements
Resource Efficient	Maximum of 5 global clocks for ×72 interface.
Good Performance	200 MHz DDR2 SDRAM on fastest speed grade.

The Cyclone III external memory interface infrastructure includes the components listed in Table 9–2.

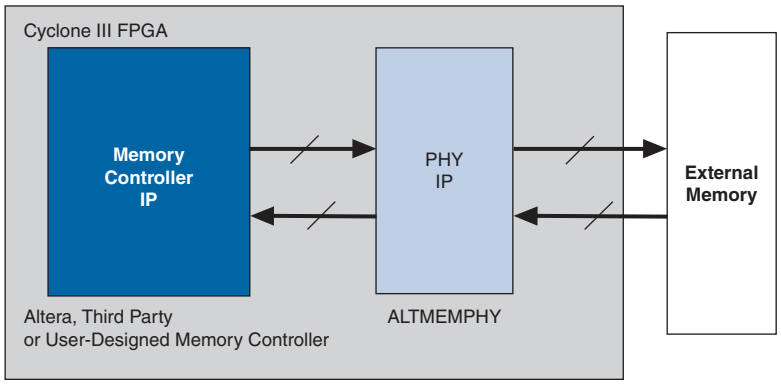
Table 9–2. Cyclone III External Memory Interface Infrastructure

Memory Interface Feature	Description
Auto-calibrating ALTMEMPHY megafunction for DDR2/DDR interfaces	Manages the physical layer (PHY) interfaces between the FPGA device and the external memory devices. It is a megafunction, which is available in the Quartus® II software version 7.0 or later.
Altera®, third party, or user-designed memory controller	Controls the PHY interface and the interface between the PHY and the user's application. The Altera controllers are included with Altera software subscriptions as part of the IP-BASE Suite.
Silicon enhancements	The phase-locked loop (PLL) reconfiguration feature adjusts the clock phase shifts in the system to calibrate changes in voltage and temperature. Two additional registers were added to Cyclone III input/output elements (IOEs) to enhance double-data rate I/O (DDIO) timing.
Quartus II Timing Analyzer and Classic Timing Analyzer	Uses industry standard synopsys design constraint (SDC) language to easily support source-synchronous timing analysis.

Altera recommends that you construct all DDR2/DDR SDRAM external memory interfaces using the Altera ALTMEMPHY megafunction. You can implement the controller function using the Altera DDR2/DDR SDRAM memory controllers, third-party controllers, or a custom controller for unique application needs. Cyclone III devices support QDRII interfaces electrically, but Altera does not supply the controller or PHY megafunctions for QDRII interfaces.

Figure 9–1 shows an overview of a Cyclone III external memory interface.

Figure 9–1. Cyclone III External Memory Interface Overview



This chapter includes a description of the hardware interfaces for external memory interfaces available in the Cyclone III devices.

For more information about implementing complete external memory interfaces, refer to the *ALTMEMPHY Megafunction User Guide*, *AN 438: Constraining and Analyzing Timing for External Memory Interfaces*, *AN 445: Design Guidelines for Implementing DDR and DDR2 SDRAM Interfaces in Cyclone III Devices*, and *DDR and DDR2 SDRAM Controller Compiler User Guide*.

This chapter contains the following sections:

- "Cyclone III Memory Support Overview"
- "Cyclone III Memory Interfaces Pin Support"
- "Cyclone III Memory Interfaces Features"

Cyclone III Memory Support Overview

This section describes the interface between Cyclone III devices and external memory standards.

Table 9–3 summarizes the maximum clock rate that Cyclone III devices can support with external memory interfaces.

Table 9–3. Cyclone III Maximum Clock Rate Support for External Memory Interfaces with Half-Rate Controller *(Note 1)*

Memory Standard	I/O Standard	Commercial									Industrial			Automotive		
		–6 Speed Grade (MHz)			–7 Speed Grade (MHz)			–8 Speed Grade (MHz)			–7 Speed Grade (MHz)			–7 Speed Grade (MHz)		
		Column I/O Banks	Row I/O Banks	Hybrid Mode	Column I/O Banks	Row I/O Banks	Hybrid Mode	Column I/O Banks	Row I/O Banks	Hybrid Mode	Column I/O Banks	Row I/O Banks	Hybrid Mode	Column I/O Banks	Row I/O Banks	Hybrid Mode
DDR2 SDRAM *(2)*	SSTL-18 Class I/II	200	167	150	167	150	133	167	133	125	167	150	133	167	133	125
DDR SDRAM *(2)*	SSTL-2 Class I/II	167	150	133	150	133	125	133	125	100	150	133	125	133	125	100
QDRII SRAM *(3)*	1.8-V HSTL Class I/II	167	167	150	150	150	133	133	133	125	150	150	133	133	133	125

Notes to Table 9–3:

(1) Column I/Os refer to top and bottom I/Os. Row I/Os refer to Right and Left I/Os. Hybrid mode refers to the combination of column and row I/Os.

(2) The values apply for interfaces with both modules and components.

(3) QDRII SRAM also supports the 1.5-V HSTL I/O standard. However, Altera recommends using the 1.8-V HSTL I/O standard for maximum performance because of the higher I/O drive strength.

Table 9–4. Cyclone III Maximum Clock Rate Support for External Memory Interfaces with Full-Rate Controller *(Note 1)*

Memory Standard	I/O Standard	Commercial						Industrial		Automotive	
		–6 Speed Grade (MHz)		–7 Speed Grade (MHz)		–8 Speed Grade (MHz)		–7 Speed Grade (MHz)		–7 Speed Grade (MHz)	
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks
DDR2 SDRAM *(2)*	SSTL-18 Class I/II	167	167	150	150	133	133	150	150	133	133
DDR SDRAM *(2)*	SSTL-2 Class I/II	167	150	150	133	133	125	150	133	133	125

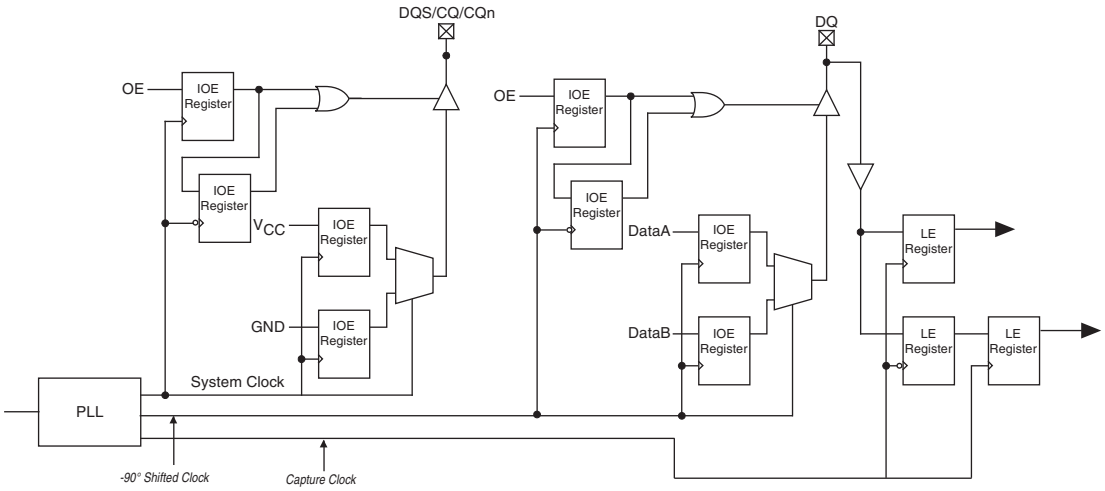
Notes to Table 9–4:

(1) Column I/Os refer to top and bottom I/Os. Row I/Os refer to right and left I/Os.

(2) The values apply for interfaces with both modules and components.

Figure 9–2 shows the block diagram of a typical external memory interface data path in Cyclone III devices.

Figure 9–2. Cyclone III External Memory Data Path *(Note 1)*



Note to Figure 9–2:

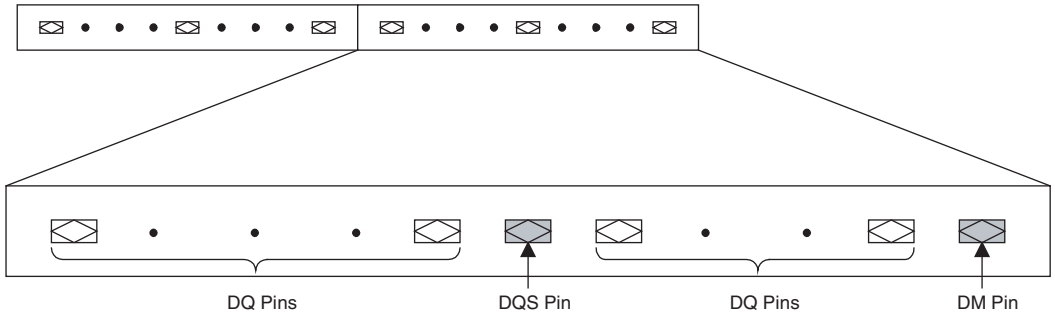
(1) All clocks shown here are global clocks.

Cyclone III Memory Interfaces Pin Support

Cyclone III devices use data (DQ), data strobe (DQS), clock, command, and address pins to interface with external memory. Some memory interfaces use the data mask (DM) or byte write select (BWS#) pins to enable data masking. This section describes how Cyclone III supports all these different pins.

Figure 9–3 illustrates the DQ and DQS pins.

Figure 9–3. Cyclone III DQ and DQS Pins *(Note 1)*, *(2)*, *(3)*, *(4)*



Notes to Figure 9–3:

(1) Each DQ group consists of a DQS pin, a DM pin, and DQ pins.

(2) DQ groups on the left and right sides of EP3C16, EP3C25, and EP3C40 (of the 240-pin PQFP package) do not support DM pin.

(3) DQ groups on the bottom sides of EP3C5, EP3C10, EP3C16, and EP3C25 (of the 144-pin EQFP package) do not support DM pin.

(4) DQ groups on the bottom sides of EP3C5, EP3C10, and EP3C16 (of the 164-pin MBGA package) do not support DM pin.

Data and Data Clock/Strobe Pins

Cyclone III data pins for external memory interfaces are called D for write data, Q for read data, or DQ for shared read and write data pins. The read-data strobes or read clocks are called DQS pins. Cyclone III devices support both bidirectional data strobes and unidirectional read clocks. Depending on the external memory standard, the DQ and DQS are bidirectional signals (in DDR2 and DDR SDRAM) or unidirectional signals (in QDRII SRAM). Connect the bidirectional DQ data signals to the same Cyclone III DQ pins. For unidirectional D or Q signals, connect the read-data signals to a group of DQ pins and the write-data signals to a different group of DQ pins.

In QDRII SRAM, the Q read-data group must be placed at a different V_{REF} bank location from the D write-data, command, or address pins.

In Cyclone III devices, DQS is used only during write mode in DDR2 and DDR SDRAM interfaces. Cyclone III devices ignore DQS as the read-data strobe because the PHY internally generates the read capture clock for read mode. However, you must connect the DQS pin to the DQS signal in DDR2 and DDR SDRAM interfaces, or to the CQ signal in QDRII SRAM interfaces.

Cyclone III does not support differential strobe pins, which is an optional feature in DDR2 SDRAM devices.

When you use the Altera Memory Controller MegaCores, the PHY is instantiated for you.

For more information about the memory interface data path, refer to the *ALTMEMPHY Megafunction User Guide*.

ALTMEMPHY is a self-calibrating megafunction, enhanced to simplify the implementation of the read-data path in different memory interfaces. The auto-calibration feature of ALTMEMPHY provides ease-of-use by optimizing clock phases and frequencies across process, voltage, and temperature (PVT) variations. You can save on the global clock resources in Cyclone III devices through the ALTMEMPHY megafunction because you do not need to route the DQS signals on the global clock buses (because DQS is ignored for read capture). Resynchronization issues do not arise because no transfer occurs from the memory domain clock (DQS) to the system domain for capturing data DQ.

All the I/O banks in Cyclone III devices support DQ and DQS signals with DQ-bus modes of ×8, ×9, ×16, ×18, ×32, and ×36. In ×8, ×16, and ×32 modes, one DQS pin drives up to 8, 16, or 32 DQ pins, respectively, within the group, to support DDR2 and DDR SDRAM interfaces.

In the ×9, ×18, and ×36 modes, a pair of DQS pins (CQ and CQ#) drives up to 9, 18, or 36 DQ pins, respectively, within the group, to support one, two, or four parity bits and the corresponding data bits. The ×9, ×18, and ×36 modes support the QDRII memory interface. CQ# is the inverted read-clock signal which is connected to the complementary data strobe (DQS/CQ#) pin. You can use any unused DQ pins as regular user I/O pins if they are not used as memory interface signals.

Table 9–5 shows the number of DQS/DQ groups supported on each side of the Cyclone III device.

Table 9–5. Cyclone III DQS and DQ Bus Mode Support for Each Side of the Device *(Note 1)* (Part 1 of 4)

Device	Package	Side	Number of ×8 Groups	Number of ×9 Groups	Number of ×16 Groups	Number of ×18 Groups	Number of ×32 Groups	Number of ×36 Groups
EP3C5	144-pin EQFP *(2)*	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top *(3)*	1	0	0	0	—	—
		Bottom *(4)*, *(5)*	1	0	0	0	—	—
	164-pin MBGA *(2)*	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top *(3)*	1	0	0	0	—	—
		Bottom *(4)*, *(5)*	1	0	0	0	—	—
	256-pin FineLine BGA/256-pin Ultra FineLine BGA *(2)*	Left *(5)*,*(6)*	1	1	0	0	—	—
		Right *(5)*, *(7)*	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
EP3C10	144-pin EQFP *(2)*	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top *(3)*	1	0	0	0	—	—
		Bottom *(4)*, *(5)*	1	0	0	0	—	—
	164-pin MBGA *(2)*	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top *(3)*	1	0	0	0	—	—
		Bottom *(4)*, *(5)*	1	0	0	0	—	—
	256-pin FineLine BGA/256-pin Ultra FineLine BGA *(2)*	Left *(5)*, *(6)*	1	1	0	0	—	—
		Right *(5)*, *(7)*	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—

Table 9–5. Cyclone III DQS and DQ Bus Mode Support for Each Side of the Device *(Note 1)* (Part 2 of 4)

Device	Package	Side	Number of ×8 Groups	Number of ×9 Groups	Number of ×16 Groups	Number of ×18 Groups	Number of ×32 Groups	Number of ×36 Groups
EP3C16	144-pin EQFP *(2)*	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top *(3)*	1	0	0	0	—	—
		Bottom *(4)*, *(5)*	1	0	0	0	—	—
	164-pin MBGA *(2)*	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top *(3)*	1	0	0	0	—	—
		Bottom *(4)*, *(5)*	1	0	0	0	—	—
	240-pin PQFP *(2)*	Left *(5)*, *(8)*	1	1	0	0	—	—
		Right *(4)*, *(5)*	1	0	0	0	—	—
		Top	1	1	0	0	—	—
		Bottom	1	1	0	0	—	—
	256-pin FineLine BGA/256-pin Ultra FineLine BGA *(2)*	Left *(5)*, *(6)*	1	1	0	0	—	—
		Right *(5)*, *(7)*	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	484-pin FineLine BGA/484-pin Ultra FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1

Table 9–5. Cyclone III DQS and DQ Bus Mode Support for Each Side of the Device *(Note 1)* (Part 3 of 4)

Device	Package	Side	Number of ×8 Groups	Number of ×9 Groups	Number of ×16 Groups	Number of ×18 Groups	Number of ×32 Groups	Number of ×36 Groups
EP3C25	144-pin EQFP *(2)*	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top *(3)*	1	0	0	0	—	—
		Bottom *(4)*, *(5)*	1	0	0	0	—	—
	240-pin PQFP *(2)*	Left *(5)*, *(8)*	1	1	0	0	—	—
		Right *(4)*, *(5)*	1	0	0	0	—	—
		Top	1	1	0	0	—	—
		Bottom	1	1	0	0	—	—
	256-pin FineLine BGA/256-pin Ultra FineLine BGA *(2)*	Left *(5)*, *(6)*	1	1	0	0	—	—
		Right *(5)*, *(7)*	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	324-pin FineLine BGA *(2)*	Left	2	2	1	1	—	—
		Right *(9)*	2	2	1	1	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
EP3C40	240-pin PQFP	Left *(5)*, *(8)*	1	1	0	0	0	0
		Right *(4)*, *(5)*	1	0	0	0	0	0
		Top	1	1	0	0	0	0
		Bottom	1	1	0	0	0	0
	324-pin FineLine BGA	Left	2	2	1	1	0	0
		Right *(9)*	2	2	1	1	0	0
		Top	2	2	1	1	0	0
		Bottom	2	2	1	1	0	0
	484-pin FineLine BGA/484-pin Ultra FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1

Table 9–5. Cyclone III DQS and DQ Bus Mode Support for Each Side of the Device *(Note 1)* (Part 4 of 4)

Device	Package	Side	Number of ×8 Groups	Number of ×9 Groups	Number of ×16 Groups	Number of ×18 Groups	Number of ×32 Groups	Number of ×36 Groups
EP3C55	484-pin FineLine BGA/484-pin Ultra FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1
EP3C80	484-pin FineLine BGA/484-pin Ultra FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1
EP3C120	484-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1

Notes to Table 9–5:

(1) These numbers are preliminary until characterization is final.

(2) This device package does not support ×32/×36 mode.

(3) For the top side of the device, RUP, RDN, PLLCLKOUT3n, and PLLCLKOUT3p pins are shared with the DQ/DM pins to gain ×8 DQ group. You cannot use these groups if you are using the RUP and RDN pins for on-chip termination (OCT) calibration or if you are using PLLCLKOUT3n and PLLCLKOUT3p.

(4) There is no DM pin support for these groups.

(5) The RUP and RDN pins are shared with the DQ pins. You cannot use these groups if you are using the RUP and RDN pins for OCT calibration.

(6) The ×8 DQ group can be formed in Bank 2.

(7) The ×8 DQ group can be formed in Bank 5.

(8) There is no DM and BWS# pins support for these groups.

(9) The RUP pin is shared with the DQ pin to gain ×9 or ×18 DQ group. You cannot use these groups if you are using the RUP and RDN pins for OCT calibration.

For more information about device package outline, refer to the Device Packaging Specifications.

The DQS pins are listed in the Cyclone III pin tables as DQSXY, where X indicates the DQS grouping number and Y indicates which side of the I/O bank the DQS pins belong. The Y can be T for pins on the top, B for pins on the bottom, L for pins on the left, or R for pins on the right side of the device. Similarly, the corresponding DQ pins are marked as DQXY, where the X denotes which DQ group the pins belong to and Y denotes the I/O bank location of the DQ pins. The Y can be T for pins on the top, B for pins on the bottom, L for pins on the left, or R for pins on the right side of the device. For example, DQS2T indicates a DQS pin belonging to group 2, located on the top side of the device. Similarly, the DQ pins belonging to that group is shown as DQ2T.

☞ Each DQ group is associated with its corresponding DQS pins, as defined in the Cyclone III pin tables; for example:

- For DDR2/DDR SDRAM, a ×8 DQ group DQ3B[7:0] pins are associated with the DQS3B pin (same 3B group index)
- For QDRII SRAM, a ×9 Q read-data group DQ3L[8..0] pins are associated with DQS2L/CQ3L and DQS3L/CQ3L# pins (same 3L group index)

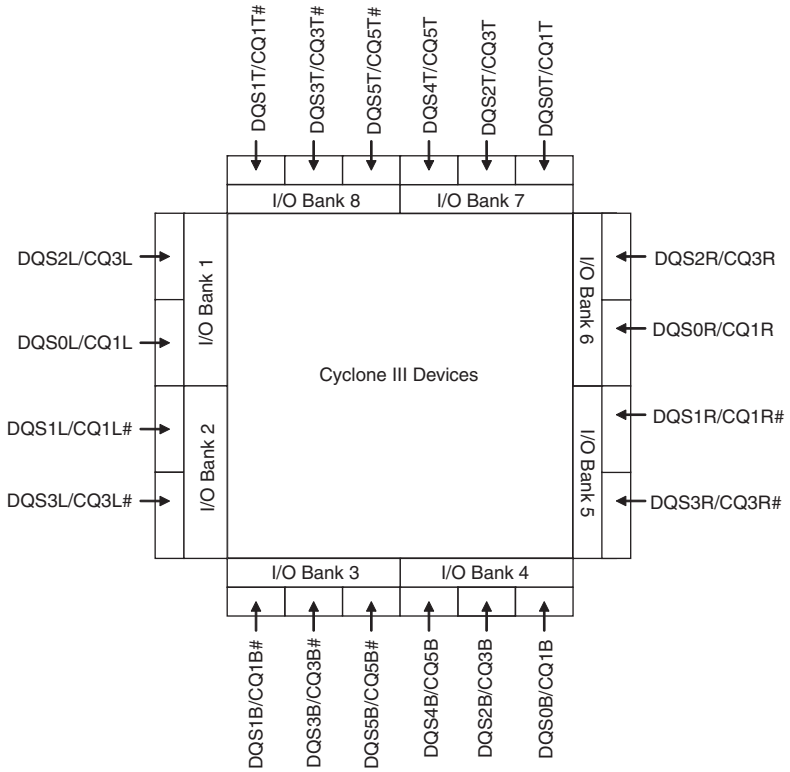
The Quartus II software issues an error message if a DQ group is not placed properly with its associated DQS.

DQ pin numbering is based on ×8/×9 mode. There are up to 20 DQS/DQ groups in ×8 mode or up to 8 DQS/DQ groups in ×9 mode in the I/O banks, that can be utilized for the external memory interface.

Figure 9–4 and Figure 9–5 show the location and numbering of the DQS/DQ/CQ# pins in the Cyclone III I/O banks.

☞ For Cyclone III memory interface support, only one interface can be placed on each side.

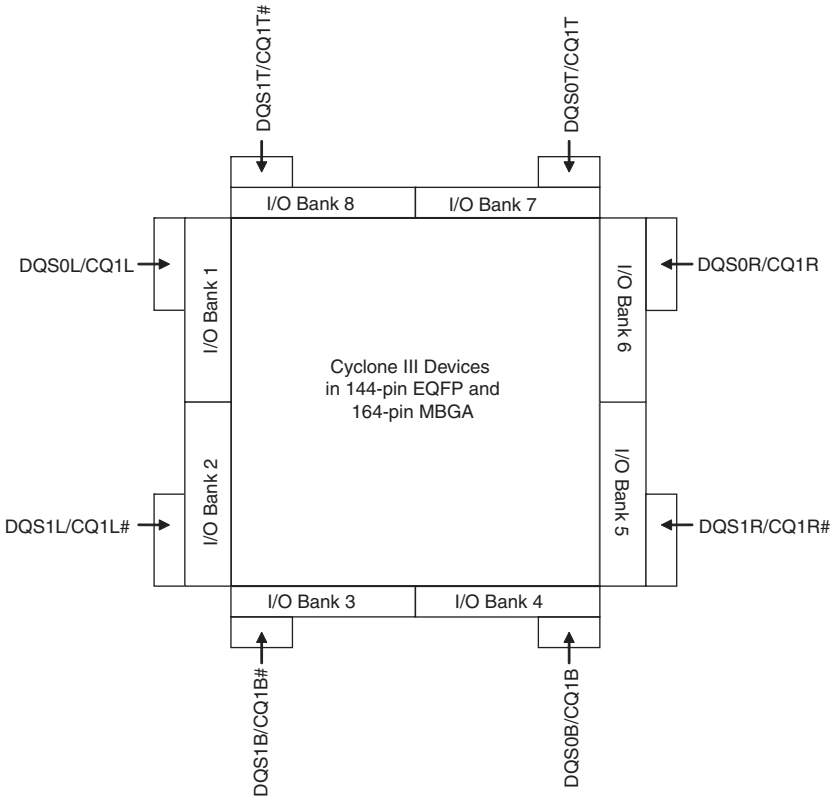
Figure 9–4. DQS/CQ/CQ# Pins in Cyclone III I/O Banks *(Note 1)*



Note to Figure 9–4:

(1) The DQS/CQ/CQ# pin locations in this diagram apply to all packages in the Cyclone III family except devices in 144-pin EQFP and 164-pin MBGA packages.

Figure 9–5. DQS/CQ/CQ# Pins for Devices in the 144-Pin EQFP and 164-pin MBGA Packages



In Cyclone III devices, the ×9 mode uses the same DQ and DQS pins as the ×8 mode, and one additional DQ pin that serves as a regular I/O pin in ×8 mode. The ×18 mode uses the same DQ and DQS pins as ×16 mode, with two additional DQ pins that serve as regular I/O pins in ×16 mode. Similarly, the ×36 mode uses the same DQ and DQS pins as ×32 mode, with four additional DQ pins that serve as regular I/O pins in ×32 mode. When not used as DQ or DQS pins, the memory interface pins are available as regular I/O pins.

Optional Parity, DM, and ECC Pins

Cyclone III devices support parity in the ×9, ×18, and ×36 modes. One parity bit is available per eight bits of data pins. You can use any of the DQ pins for parity in the Cyclone III devices because the parity pins are treated and configured like DQ pins.

The data mask (DM) pins are only required when writing to DDR2 and DDR SDRAM devices. QDRII SRAM devices use the BWS# signal to select the byte to be written into memory. A low signal on the DM or BWS# pin indicates the write is valid. Driving the DM or BWS# pin high causes the memory to mask the DQ signals. Each group of DQS and DQ signals has one DM pin. Similar to the DQ output signals, the DM signals are clocked by the –90° shifted clock.

In Cyclone III devices, the DM pins are preassigned in the device pinouts. The Quartus II Fitter treats the DQ and DM pins in a DQS group equally for placement purposes. The preassigned DQ and DM pins are the preferred pins to use.

Some DDR2 SDRAM and DDR SDRAM devices support error correction coding (ECC), a method of detecting and automatically correcting errors in data transmission. In 72-bit DDR2 or DDR SDRAM, there are eight ECC pins and 64 data pins. Connect the DDR2 and DDR SDRAM ECC pins to a DQS/DQ group in Cyclone III devices. The memory controller needs additional logic to encode and decode the ECC data.

Address and Control/Command Pins

The address signals and the control or command signals are typically sent at a single data rate. You can use any of the user I/O pins on all I/O banks of Cyclone III devices to generate the address and control or command signals to the memory device.

☞ Cyclone III devices do not support QDRII SRAM in the burst length of two.

Memory Clock Pins

In DDR2 and DDR SDRAM memory interfaces, the memory clock signals (CK and CK#) are used to capture the address signals and the control or command signals. Similarly, QDRII SRAM devices use the write clocks (K and K#) to capture the address and command signals. The CK/CK# and K/K# signals are generated to mimic the write-data strobe using the DDIO registers in Cyclone III devices. You can use any regular adjacent I/O pins (preferably differential I/O pair) to generate the CK/CK# for DDR2 and DDR SDRAM interface or K/K# for QDRII SRAM.

Cyclone III Memory Interfaces Features

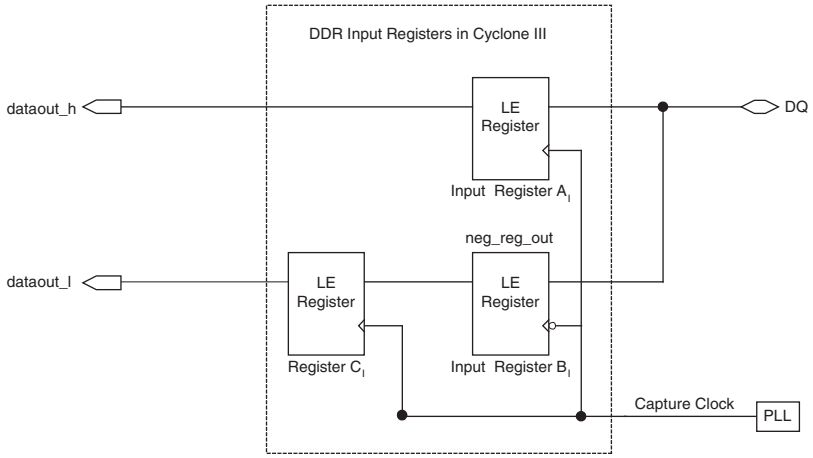
In this section, Cyclone III memory interfaces, including DDR input registers, DDR output registers, OCT, and PLLs, are discussed.

DDR Input Registers

The DDR input registers are implemented with three internal logic element (LE) registers for every DQ pin. These LE registers are located in the logic array block (LAB) adjacent to the DDR input pin.

Figure 9–6 illustrates the Cyclone III DDR input registers.

Figure 9–6. Cyclone III DDR Input Registers



The DDR data is first fed to two registers, input register A_I and input register B_I.

- Input register A_I captures the DDR data present during the rising edge of the clock
- Input register B_I captures the DDR data present during the falling edge of the clock
- Register C_I aligns the data before it is synchronized with the system clock

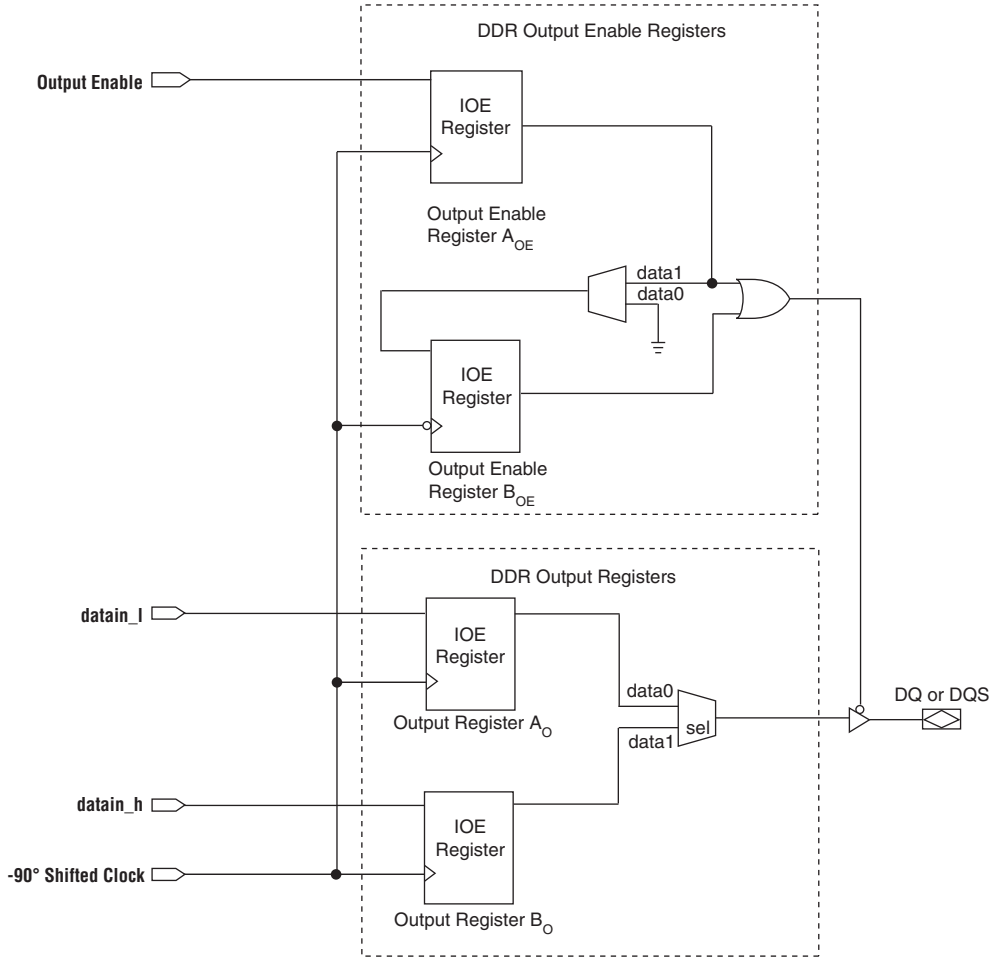
The data from the DDR input register is fed to two registers, `sync_reg_h` and `sync_reg_l`, then the data is transferred to a FIFO block to synchronize the two data streams to the rising edge of the system clock. Since the read-capture clock is generated by the PLL, the read-data strobe signal (`DQS` or `CQ`) is not used during read in Cyclone III devices. Hence, postamble is not a concern in this case.

DDR Output Registers

A dedicated write DDIO block is implemented in the DDR output and output enable paths.

Figure 9–7 shows how the Cyclone III dedicated write DDIO block is implemented in the IOE registers.

Figure 9–7. Cyclone III Dedicated Write DDIO



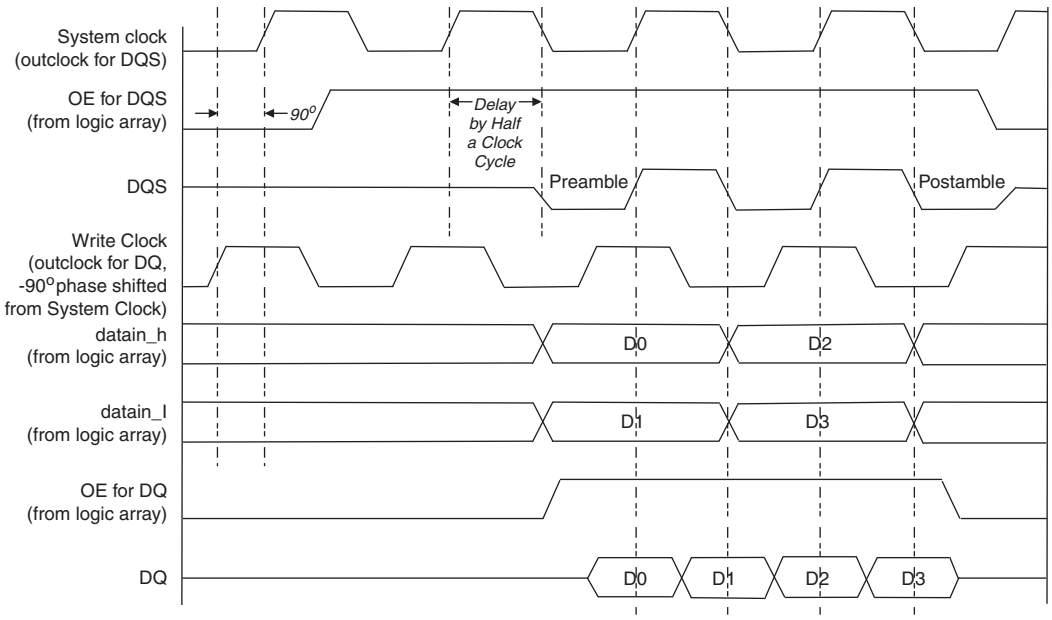
The two DDR output registers are located in the I/O element (IOE) block. Two serial data streams routed through `datain_l` and `datain_h` are fed into two registers, `output register Ao` and `output register Bo`, respectively, on the same clock edge. The output from `output register Ao` is captured on the falling edge of the clock, while the output from `output register Bo` is captured on the rising edge of the clock. The registered outputs are multiplexed by the common clock to drive the DDR output pin at twice the data rate.

The DDR output enable path has a similar structure to the DDR output path in the IOE block. The second output enable register provides the write preamble for the `DQS` strobe in DDR external memory interfaces. This active-low output enable register extends the high-impedance state of the pin by half a clock cycle to provide the external memory's `DQS` write preamble time specification.

For more information about the Cyclone III IOE registers, refer to the *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*.

Figure 9–8 illustrates how the second output enable register extends the DQS high-impedance state by half a clock cycle during a write operation.

Figure 9–8. Extending the OE Disable by Half a Clock Cycle for a Write Transaction *(Note 1)*



Note to Figure 9–8:

(1) The waveform reflects the software simulation result. The OE signal is an active low on the device. However, the Quartus II software implements the signal as an active high and automatically adds an inverter before the A_{OE} register D input.

On-Chip Termination (OCT)

Cyclone III supports calibrated on-chip series termination (Rs OCT) in both vertical and horizontal I/O banks. To use the calibrated OCT, you need to use the RUP and RDN pins for each Rs OCT control block (one for each side). You can use each OCT calibration block to calibrate one type of termination with the same V_{CCIO} for that given side.

For more information about the Cyclone III OCT calibration block, refer to the *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*.

PLL

When interfacing with external memory, the PLL is used to generate the memory system clock, the write clock, the capture clock, and the logic-core clock. The system clock generates the DQS write signals, commands, and addresses. The write-clock is shifted by –90° from the system clock and generates the DQ signals during writes. You can use the PLL reconfiguration feature to calibrate the read-capture phase shift to balance the setup and hold margins.

The PLL is instantiated within the ALTMEMPHY megafunction. All the outputs of the PLL are used when the ALTMEMPHY megafunction is instantiated to interface with external memories.

For more information about usage of PLL outputs by the ALTMEMPHY megafunction, refer to the *ALTMEMPHY Megafunction User Guide*.

For more information about the Cyclone III PLL, refer to the *Clock Networks and PLLs in Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

Conclusion

Cyclone III devices support DDR2 SDRAM, DDR SDRAM, and QDRII SRAM external memory interfaces. The self-calibrating ALTMEMPHY megafunction simplifies the implementation of data paths for DDR2 and DDR memory interfaces and dynamically calibrates out the process, voltage, and temperature variations in Cyclone III devices and external memory devices without interrupting normal operation.

Cyclone III allows a transfer data rate between external memory interfaces of up to 200 MHz/400 Mbps for DDR2 SDRAM, 167 MHz/333 Mbps for DDR SDRAM, and 167 MHz/667 Mbps for QDRII SRAM devices.

Cyclone III devices also offer dedicated write DDIO registers to improve the output duty cycle and provide a better write margin.

Referenced Documents

This chapter references the following documents:

- *ALTMEMPHY Megafunction User Guide*
- *AN 438: Constraining and Analyzing Timing for External Memory Interfaces in Stratix III and Cyclone III Devices*
- *AN 445: Design Guidelines for Implementing DDR & DDR2 SDRAM Interfaces in Cyclone III Devices*
- *Clock Networks and PLLs in Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*
- *DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*
- *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*
- *DDR and DDR2 SDRAM Controller Compiler User Guide*
- *Logic Elements and Logic Array Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Memory Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*
- *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*

Document Revision History

Table 9–6 shows the revision history for this chapter.

Table 9–6. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
October 2008 v1.3	■ Updated "Introduction" section ■ Updated "DDR Input Registers" section ■ Updated "Conclusion" section ■ Updated chapter to new template	—
May 2008 v1.2	■ Added *(Note 4)* to Figure 9–3 ■ Updated Table 9–3 ■ Added new Table 9–4 ■ Updated Table 9–5 ■ Updated *(Note 1)* to Figure 9–4 ■ Updated Figure 9–5 and 9–14	—
July 2007 v1.1	■ Updated "Data and Data Clock/Strobe Pins" section ■ Updated Table 9–5 ■ Added chapter TOC and "Referenced Documents" section	—
March 2007 v1.0	Initial release.	—

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